[ENGLISH TRANSLATION]

Japanese Patent Laid-Open No. **63-10558**
Laid-Open Date: January 18, 1988
Application No. 61-154026
Application Date: July 2, 1986
Request for Examination: Not Made
IPC's: H01L 27/12, G02F 1/133, G09F 9/30
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Continue to the last page.

SPECIFICATION

1. Title of the Invention: FLAT DISPLAY

2. Claims

[Claim 1] A flat display having a display element and an active element arranged in each area surrounded by a scanning line and a signal line arrayed in a matrix to form each pixel, characterized in that a switching element is provided between said each scanning line and signal line and an earth line.

[Claim 2] The flat display according to Claim 1, characterized in that the threshold voltage of said switching element is higher than the on-state voltage of the active element.

[Claim 3] The flat display according to Claim 1, characterized in that said switching element works in both positive and negative directions with respect to driving voltage.

3. Detailed Description of the Invention

[Technical Field of the Invention]

The present invention relates to a flat display for a

liquid crystal display and so on, and more particularly, to a flat display of active matrix type in which each display element is provided with an active element.

[Prior Art]

Conventionally, while cathode-ray tubes have been widely used as devices for displaying characters, graphics, or TV images, recently, dot-matrix type displays using a liquid crystal or EL are receiving much attention because of advantages of reducing the depth of a display. However, in such dot-matrix type displays, when the number of dots (pixels) is increased in order to obtain resolution equal to that of the cathode-ray tube, crosstalk occurs, particularly in the case of time-sharing liquid crystal display, extremely degrading the contrast of the images. In order to avoid it, there is proposed and is being developed a so-called active matrix type display in which each pixel is provided with a switching element, such as a thin-film transistor (hereinafter, abbreviated to a TFT) and a thin-film diode.

As a conventional art specifically relating to this type of displays, the Sep. 10, 1984 issue of Nikkei Electronics, No. 351, pp. 211-240, is well known, in which a technique of flat color display having a switching thin-film transistor (TFT) in a liquid-crystal color panel is described.

More specifically, such a display is configured such that a gate line 1 and a drain line 2 are arrayed to cross each other in a matrix, as shown in Fig. 7, so that the switching of each display element 3 arranged in each area surrounded by each lines 1 and 2 is driven by each active element 4. When the active element 4 is turned on, the display element 3 displays image information, and when turned off, it holds the information.

[Problems that the Invention is to Solve]

However, the flat display with such a configuration has a problem of breakdown or degradation in quality of the active element 4 because of static electricity generating at

the mounting and demounting time to a panel or in the process.

Accordingly, it is an object of the present invention to provide a flat display capable of protecting an active element from electrostatic breakdown.

[Means for Solving the Problem]

According to an embodiment of the present invention, there is provided a flat display in which the electrostatic breakdown of an active element is avoided by providing a gate line and a drain line with protective transistors for conducting static electricity to the ground.

[Operation]

In the protective transistor of the invention, when static electricity is applied, the gate is turned on, and the transistor is conducted

[Embodiments of the Invention]

Referring to the drawings, embodiments of the present invention will be described hereinbelow.

Fig. 1 is a circuit block diagram showing an embodiment of a flat display according to the present invention. In the drawing, reference symbol X denotes a scanning line, Y denotes a signal line, TFT denotes a thin-film transistor as an active element, and LC denotes a display element such as a liquid-crystal display element, one thin-film transistor TFT and one display element LC constituting one pixel PIX. The pixels PIXs are connected in the form of a matrix between the scanning line X and the signal line Y, thus constituting a panel PNL of a liquid crystal display LCD.

Reference symbol LVS indicates an LCD vertical scanning circuit, which applies a scanning switching signal to a gate electrode of each thin-film transistor TFT via each scanning line X. Reference symbol LHS designates an LCD horizontal scanning circuit, which selectively applies a video signal sequentially to source and drain electrodes of the thin-film transistor TFT. Reference symbol E denotes an earth line formed on the periphery of the panel PNL, reference symbol

TFT1 denotes a first protective thin-film transistor connected between each signal line Y and the earth line E, and reference symbol TFT2 denotes a second protective thin-film transistor connected between each scanning line X and the earth line E.

Assuming that the pattern width of a source electrode S and a drain electrode D formed on a gate electrode G via an unillustrated semiconductor film such as an SiN insulating film and a-Si is W (channel width) and the distance between both electrodes S and D is L (channel length), as shown in the plan view of an essential part of Fig. 2, such protective thin-film transistors TFT1 and TFT2 each have a pattern size W/L as large as about 500/10 μm as compared with W/L ≈ 50/10 μm of the aforesaid thin-film transistor TFT as an active element, thereby having low impedance. Also, in the protective thin-film transistors TFT1 and TFT2, the earth line E and the scanning line X are formed in a chromium wiring pattern on a glass substrate SUB, as shown in Fig. 4, on which a silicon nitride film SIN, an amorphous silicon film ASI and the like are deposited; only the amorphous silicon ASI at a necessary part is patterned; and subsequently, the signal line Y on the silicon nitride film SIN, the earth line E, and the gate electrode of the protective thin-film transistor TFT2 are formed of a multilayer of chromium and aluminium.

In such a configuration, in the first and second protective thin-film transistors TFT1 and TFT2, their gate electrodes and the drain electrodes are both used as gate electrodes, and the source electrodes connect to the earth line E. Accordingly, when high voltage such as static electricity is applied to the scanning line X and the signal line Y, the thin-film transistors TFT1 and TFT2 are turned on and are conducted with the earth line E, and the thin-film transistor TFT is thus protected as an active element. In this case, the thin-film transistor TFT is turned on at

signal voltage V_D = 10V and its signal current Id = about 100 μA, and its leakage resistance is about 10^5 Ω. In this case, since the fanout of the driving circuit LVS or LHS is normally 100 μA or more, there is no problem in transmitting a signal.

Fig. 5 is a circuit block diagram showing another embodiment of the flat display according to the invention. The same elements as those of Fig. 1 are denoted by the same reference numerals. In the drawing, the different point from Fig. 1 is that a third protective thin-film transistor TFT3, which is inversely biased with respect to the first protective thin-film transistor TFT1, connects in parallel between each signal line Y and the earth line E; and a fourth protective thin-film transistor TFT4, which is inversely biased with respect to the second protective thin-film transistor TFT2, connects in parallel between each scanning line X and the earth line E. Such protective thin-film transistors TFT3 and TFT4 have completely equal pattern configuration and threshold voltage V_T to the aforesaid first and second protective thin-film transistors TFT1 and TFT2.

In such a configuration, even if high voltage such as static electricity of different polarity, positive and negative, is applied to the scanning line X, the signal line Y, the panel PNL and so on, either the first and second protective thin-film transistors TFT1 and TFT2 being operated at positive bias or the third and fourth protective thin-film transistors TFT3 and TFT4 being operated at negative bias are tuned on, and the high voltage is thus conducted to the earth line E, so that the thin-film transistor TFT as an active element can be protected.

Fig. 6 is a circuit block diagram showing another embodiment of the flat display according to the invention. The same elements as those of Fig. 1 are denoted by the same reference numerals. In this case, threshold voltage V_T of protective thin-film transistors TFT5 and TFT6 are as large

as V_T > 15V, as shown in Fig. 3; accordingly, even if normal driving voltage is applied to the scanning line X and the signal line Y, the protective thin-film transistors TFT1 or TFT2 is not turned on. Therefore, there is an advantage of reducing power consumption of the vertical scanning circuit LVS or the horizontal scanning circuit LHS. On the other hand, when a voltage of several KV, such as of static electricity, is applied, the protective thin-film transistors TFT5 and TFT6 are turned on, and therefore the protective thin-film transistors TFT1 and TFT2 are also turned on, so that the energy of static electricity can be grounded.

[Advantage of the Invention]

According to the invention, as described above, since the flat display having the display element and the active element arranged in each area surrounded by the scanning line and the signal line arrayed in a matrix to form each pixel includes the switching element between the scanning line and the signal line and the earth line, electrostatic breakdown of the active element can be prevented reliably, thereby obtaining a remarkable advantage of providing a flat display of high quality and reliability.

4. Brief Description of the Drawings

Fig. 1 is a plan view showing an embodiment of a flat display according to the present invention; Fig. 2 is a plan view explaining the configuration of a thin-film transistor; Fig. 3 is an explanatory view of the characteristic of the thin-film transistor; Fig. 4 is a perspective view of an essential part showing the configuration of the flat display according to the invention; Figs. 5 and 6 are plan views each showing another embodiment of the flat display according to the invention; and Fig. 7 is a plan view of an essential part explaining a conventional flat display.

X: scanning line, Y: signal line, PIX: pixel, LCD: liquid crystal display, PNL: panel, LC: liquid-crystal display element, E: earth line, LHS: LCD horizontal scanning circuit,

LVC: LCD vertical scanning circuit, TFT: thin-film transistor, TFT1, TFT2, TFT3, TFT4, TFT5, TFT6: protective thin-film transistor

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[Fig. 1]
X: scanning line
Y: signal line
E: earth line
LC: liquid crystal element
TFT: thin-film transistor
PIX: pixel
PNL: panel
LCD: liquid crystal display
TFT1: protective thin-film transistor
TFT2: protective thin-film transistor
LHS: LCD horizontal scanning circuit
LVS: LCD vertical scanning circuit
1: LCD horizontal scanning circuit
2: LCD vertical scanning circuit
[Fig. 3]
1: drain current
2: gate current
[Fig. 5]
1: LCD horizontal scanning circuit
2: LCD vertical scanning circuit
[Fig. 6]
1: LCD horizontal scanning circuit
2: LCD vertical scanning circuit

Continued from page 1
IPC's: H01L 29/78
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[Type of Gazette] Publication of Amendment According to Article 17-2 of Patent Law
[Classification] Group 2 in Section 6
[Date of Publication] June 24, 1994
[Laid-Open Number] Japanese Patent Laid-Open No. 10558/1988
[Laid-Open Date] January 18, 1988
[Issue in Year] Publication of Unexamined Patent Application 63-106
[Application Number] Japanese Patent Application No. 154026/1986
[International Patent Classification, Ver. 5]
G02F 1/136 500 9018-2K
1/133 550 9226-2K
H01L 29/784
[F1]
H01L 29/78 311 A 9056-4M

Written Amendment (Voluntary)
Director General of Patent Office, Esq.
June 30, 1993
Designation of the Case
Japanese Patent Application No. 164026/1986
Title of the Invention
Flat Display
Party Effecting the Amendment
Connection with the Case: Applicant of the Invention
Name: (510) Hitachi Ltd.
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Object of Amendment

Claims and Detailed Description of the Invention in Specification

Amendment Details

1. The claims are amended as the attached paper.

2. The following description will be added to the end of line 2 on page 4 of the application specification: In addition, while there is a known art regarding the protective transistor for the TFT disclosed in Japanese Patent Laid-Open No. 79259/1986, there is no description of bringing the threshold voltage of the protective transistor shown in Fig. 3 larger than the threshold value of the active element. Also, while Japanese Patent Laid-Open No. 86587/1985 describes that a bidirectional conductive transistor is used for a protective transistor, there is no description that the positive and negative protective transistors, shown in Fig. 5, are connected in parallel to form a bidirectional transistor.

Attachment

Claims:

[Claim 1] A flat display having a display element and an active element arranged in each area surrounded by a scanning line and a signal line arrayed in a matrix to form each pixel, characterized in that a switching element is provided between said each scanning line and signal line and an earth line and the threshold voltage of said switching element is larger than the on-state voltage of the active element.

[Claim 2] The flat display according to Claim 1, characterized in that said switching element includes a positive switching element and a negative switching element in parallel and works in both positive and negative directions with respect to driving voltage.